

PAT-NO: JP403249888A

DOCUMENT-IDENTIFIER: JP 03249888 A

TITLE: IMAGE MEMORY CIRCUIT

PUBN-DATE: November 7, 1991

INVENTOR-INFORMATION:

NAME

TAKAHASHI, HIROSHI

ASSIGNEE-INFORMATION:

NAME

NEC CORP

COUNTRY

N/A

APPL-NO: JP02047647

APPL-DATE: February 27, 1990

INT-CL (IPC): H04N005/92, H04N005/907

ABSTRACT:

PURPOSE: To obtain an economical image memory circuit by using one display screen quantity by constituting the circuit so that the start time for writing image data in a second image memory can be set arbitrarily in accordance with a read-out timing.

CONSTITUTION: The circuit is provided with a first image memory 1, and a second image memory having the memory capacity which becomes one display screen capacity at the time when it is added to the memory capacity of a first image memory 1. A timing control means 5 takes a synchronization of the read-out timing of a first image memory 1 and the write timing to a second image memory 3, and also, corrects the read-out timing and the write timing by a time base conversion. In such a way, an economical image memory circuit in which the image memory capacity is one display screen capacity can be obtained.

COPYRIGHT: (C)1991,JPO&Japio

----- KWIC -----

Abstract Text - FPAR (2):

CONSTITUTION: The circuit is provided with a first image memory 1, and a second image memory having the memory capacity which becomes one display screen capacity at the time when it is added to the memory capacity of a first image memory 1. A timing control means 5 takes a synchronization of the read-out timing of a first image memory 1 and the write timing to a second image memory 3, and also, corrects the read-out timing and the write timing by a time base conversion. In such a way, an economical image memory circuit in which the image memory capacity is one display screen capacity can be obtained.